

REPLACEMENT SHEET  
Ricky S. Amos et al./LUJ  
FIS920020157US1

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Pre high temp processes:

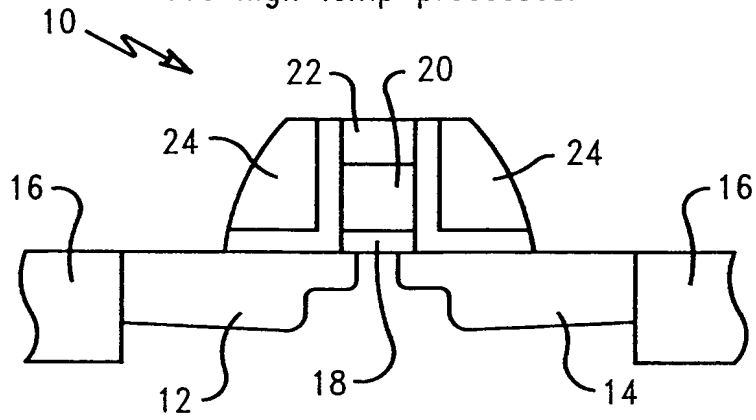


FIG. 1A

Post high temp processes:

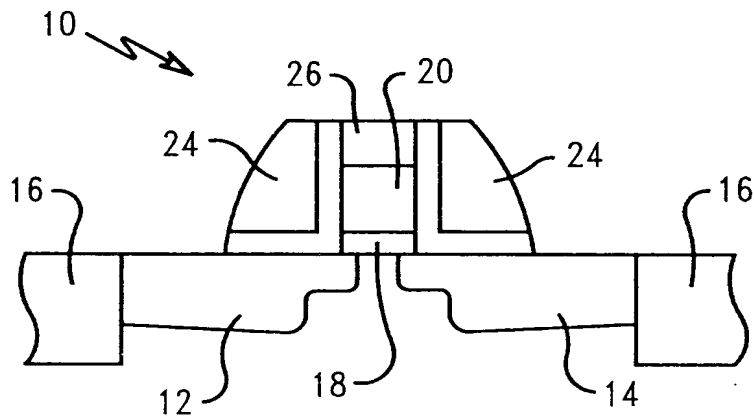
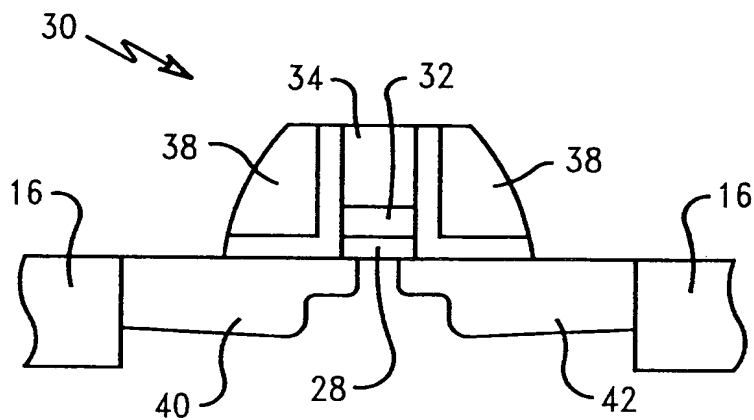
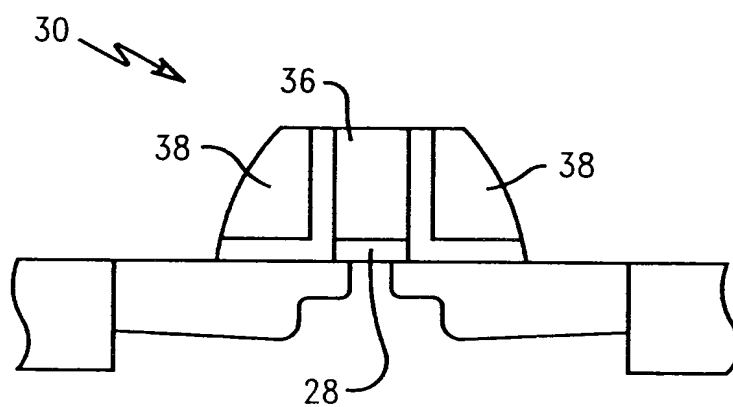


FIG. 1B



**FIG. 2A**

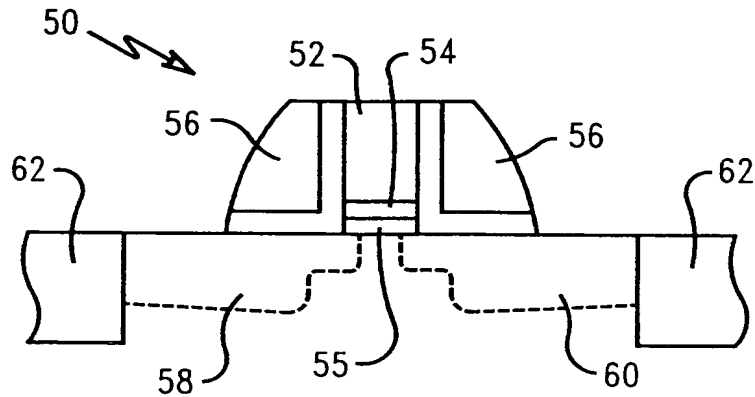
Pre high temp processes:



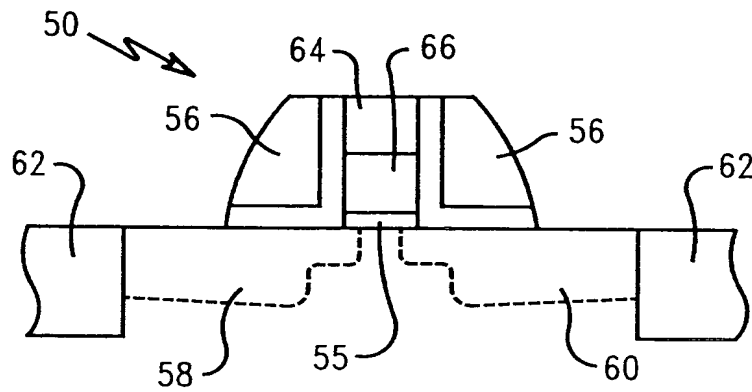
**FIG. 2B**

Post high temp processes:

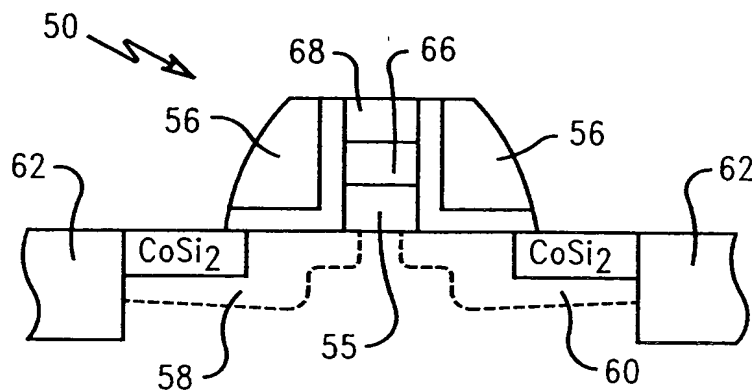
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Pre high temp processes:

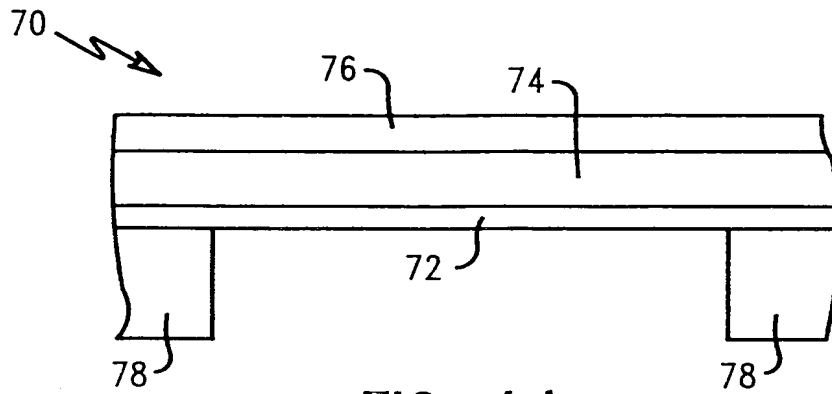


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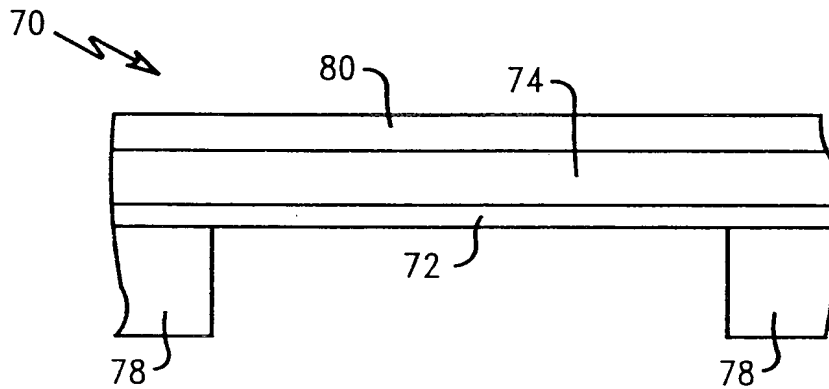


Post source/drain/gate silicide (assumed  $\text{CoSi}_2$ )

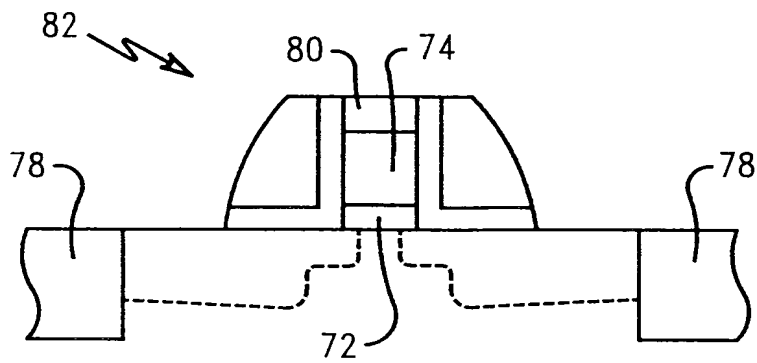
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**FIG. 4A**  
Pre silicide formation:



**FIG. 4B**  
Post silicide formation:



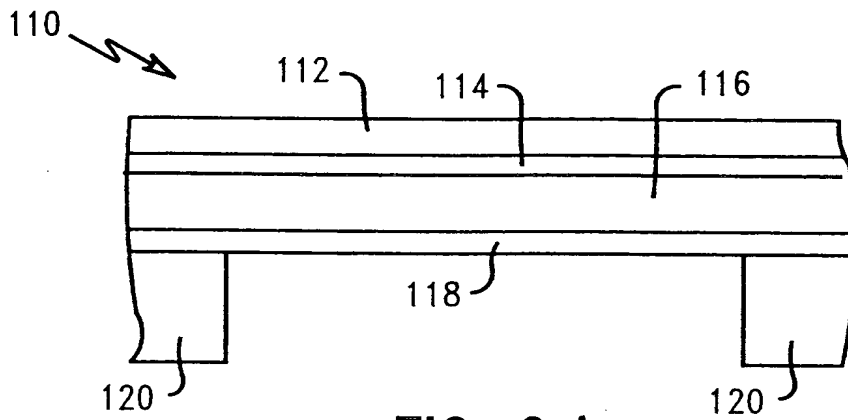
**FIG. 4C**  
Post high temp processes:

A cross-sectional view of a semiconductor device. A substrate 90 is shown at the bottom. On top of the substrate, there are two rectangular regions labeled 100. Between these regions and above them is a layer labeled 98. Above layer 98 are two horizontal layers labeled "Silicide 1" and "Silicide 2".

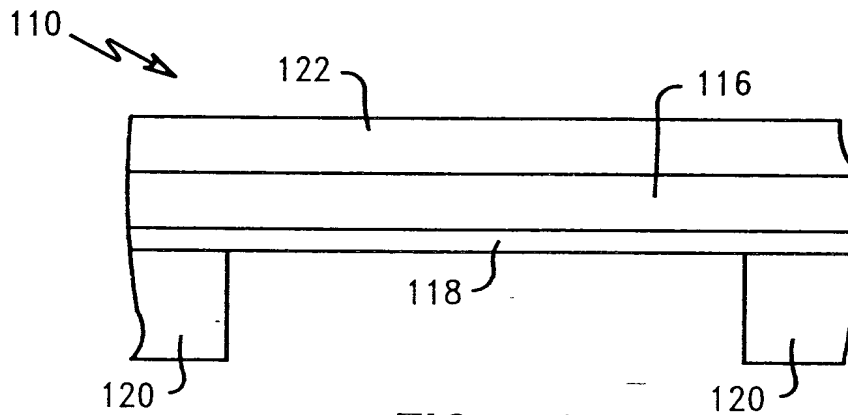
A cross-sectional view of a semiconductor device. A central gate stack is formed on a substrate 100. The gate stack includes a gate dielectric 96, a gate electrode 102, and a conductive layer 104. The gate electrode 102 is labeled "Silicide 1" and the conductive layer 104 is labeled "Silicide 2". The gate stack is flanked by side spacers 104. The substrate 100 is shown with a dashed line 98 indicating a trench or gap. The substrate 100 is also labeled with 106 and 108 at the bottom corners.

**FIG. 5C**  
Post high temp processes:

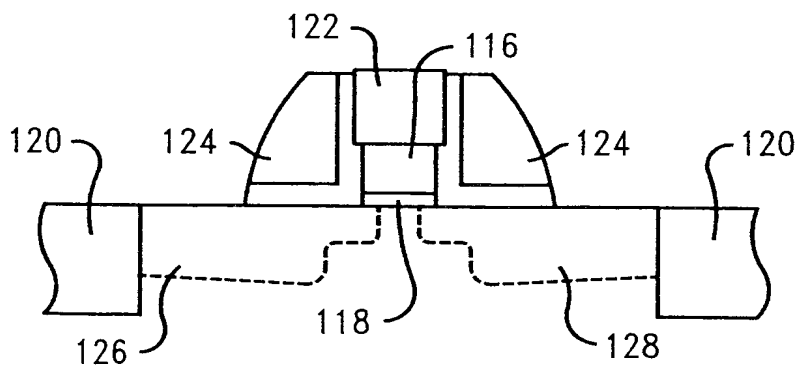
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**FIG. 6 A**  
Pre silicide formation:



**FIG. 6 B**  
Post silicide formation:



**FIG. 6 C**  
Post high temp processes:

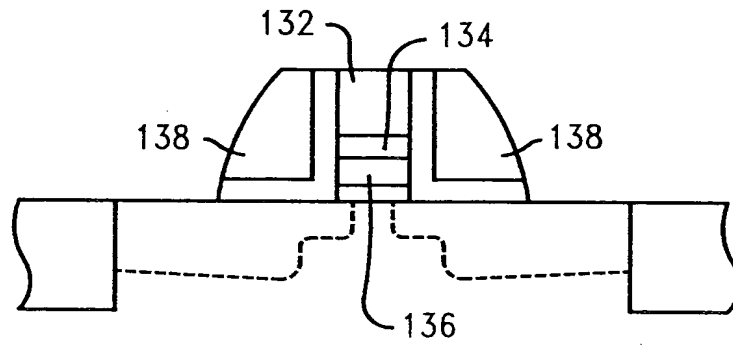


FIG. 7

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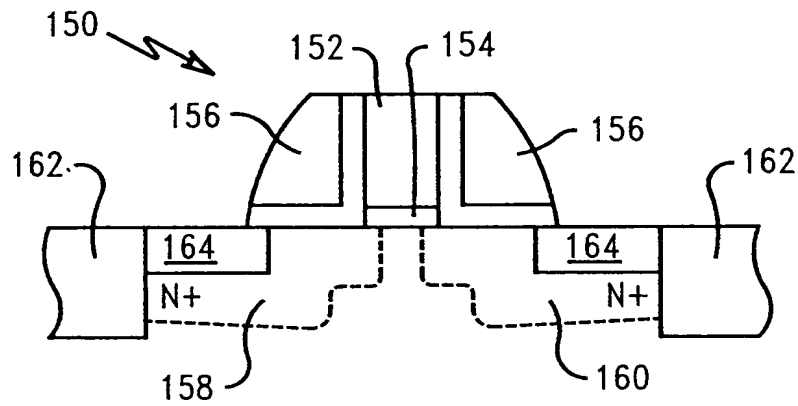


FIG. 8A

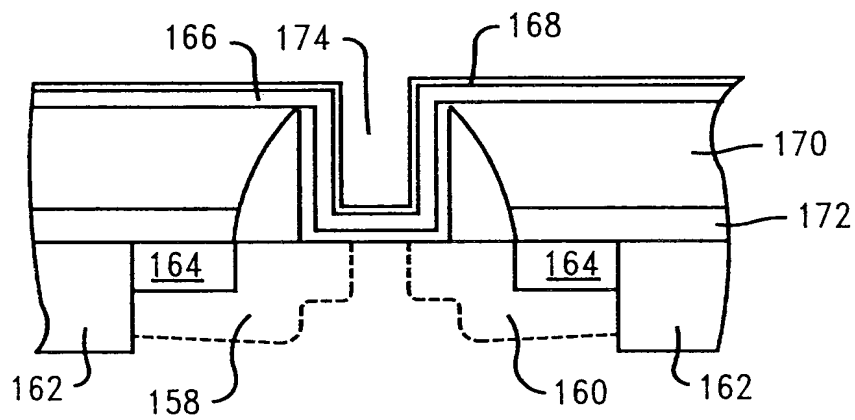


FIG. 8B



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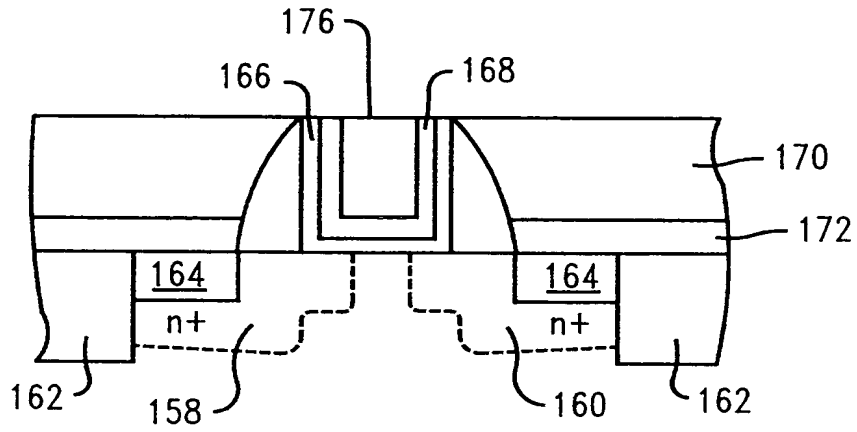


FIG. 8C

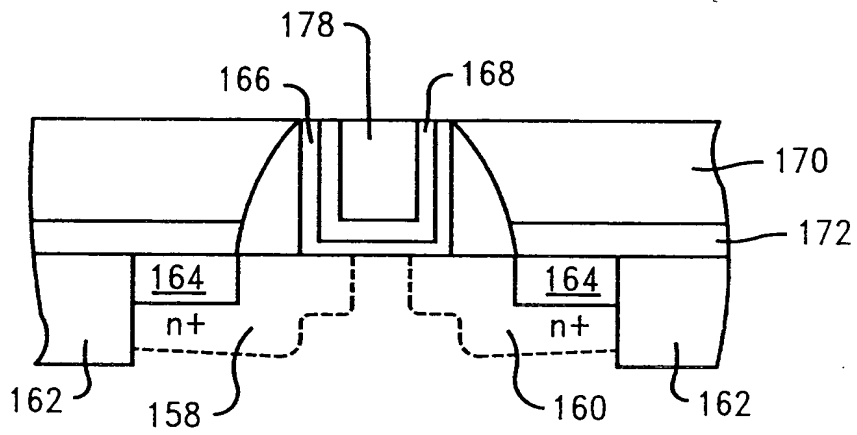


FIG. 8D

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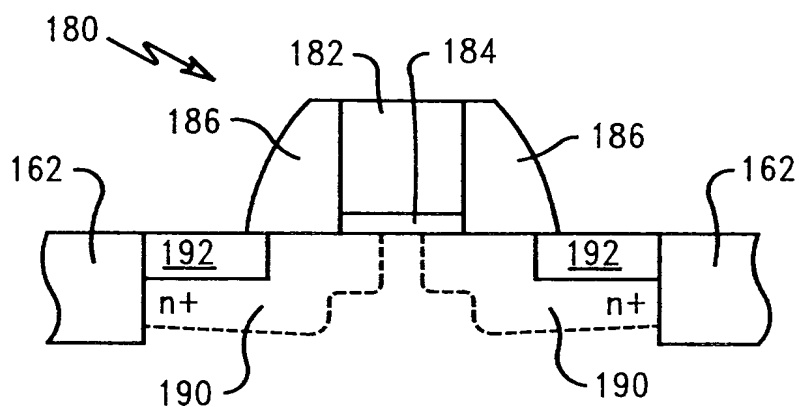


FIG. 9A

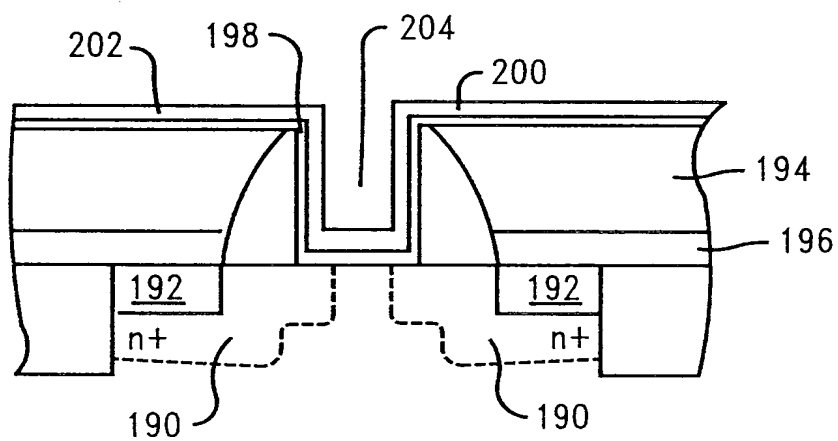


FIG. 9B

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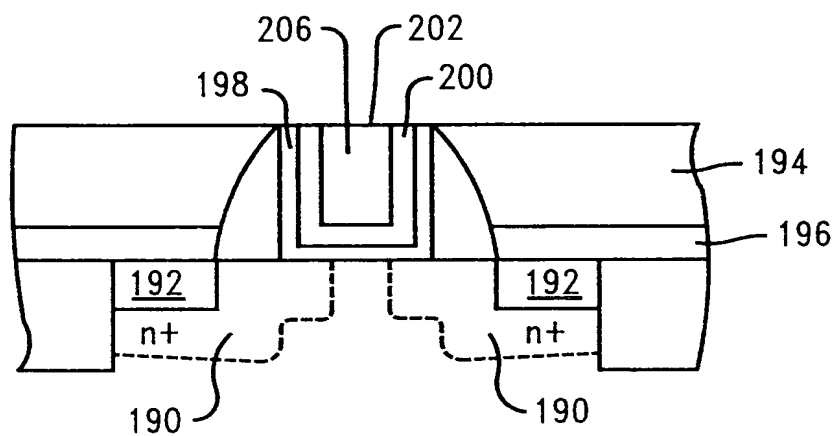


FIG. 9 C

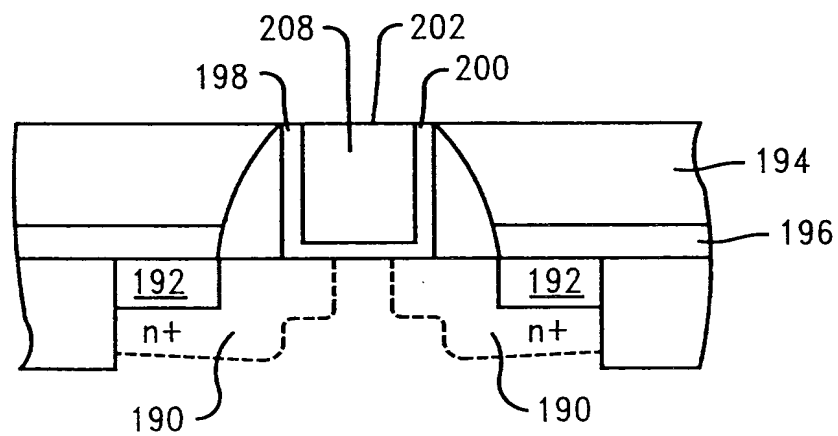


FIG. 9 D

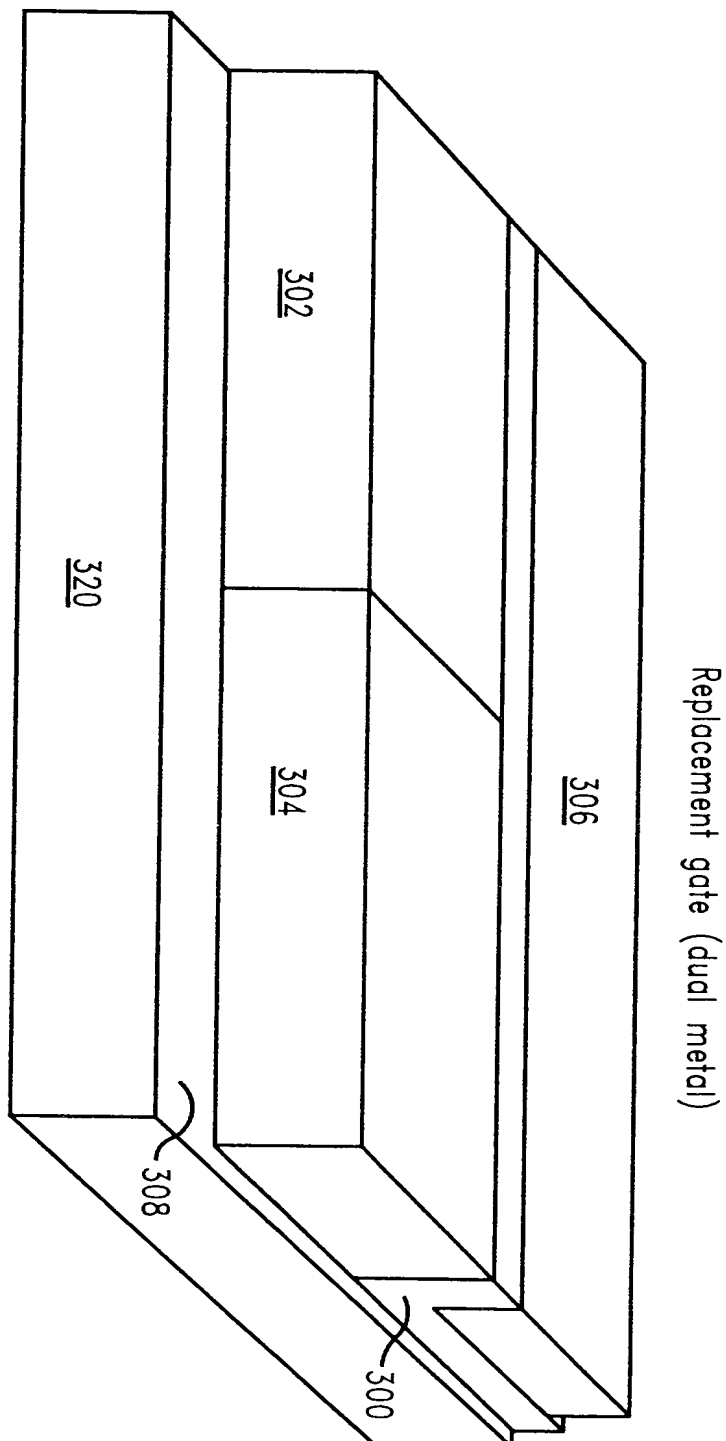


FIG. 10A

Replacement gate (dual metal)  
-> Undoped Poly-Si deposition + CMP

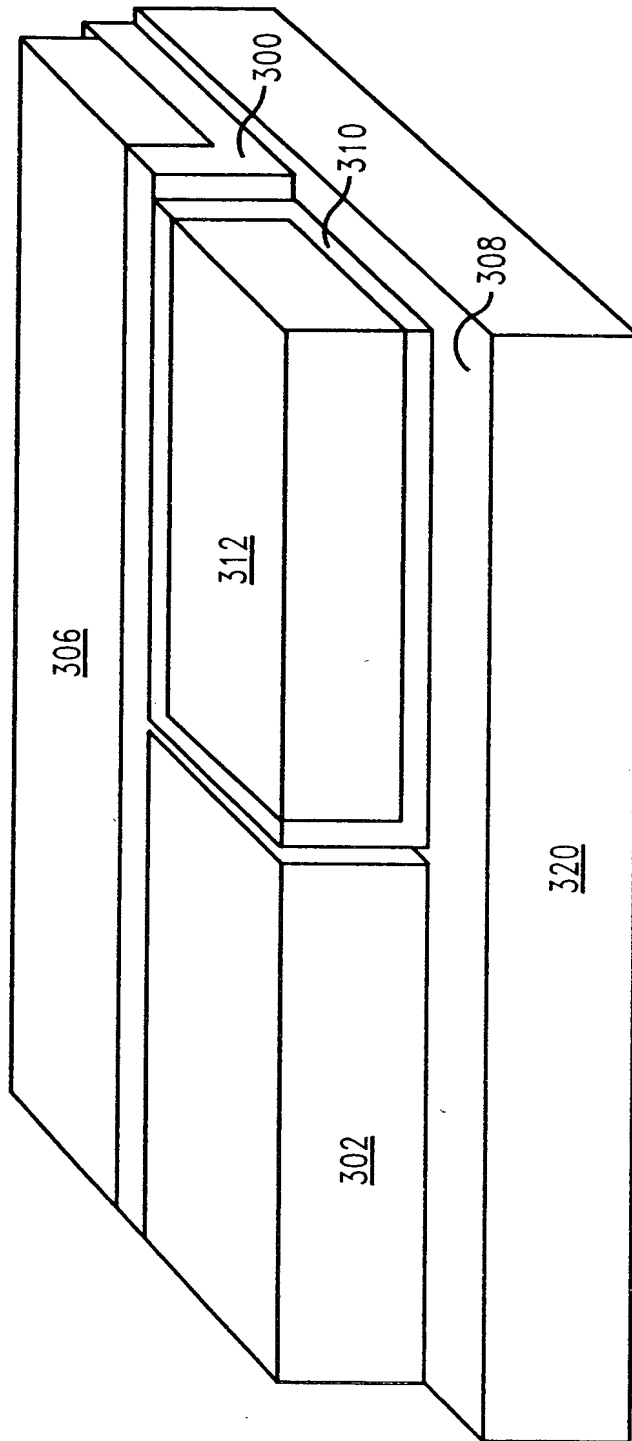


FIG. 10B

Replacement gate (dual metal)  
-> Undoped Poly deposition + CMP

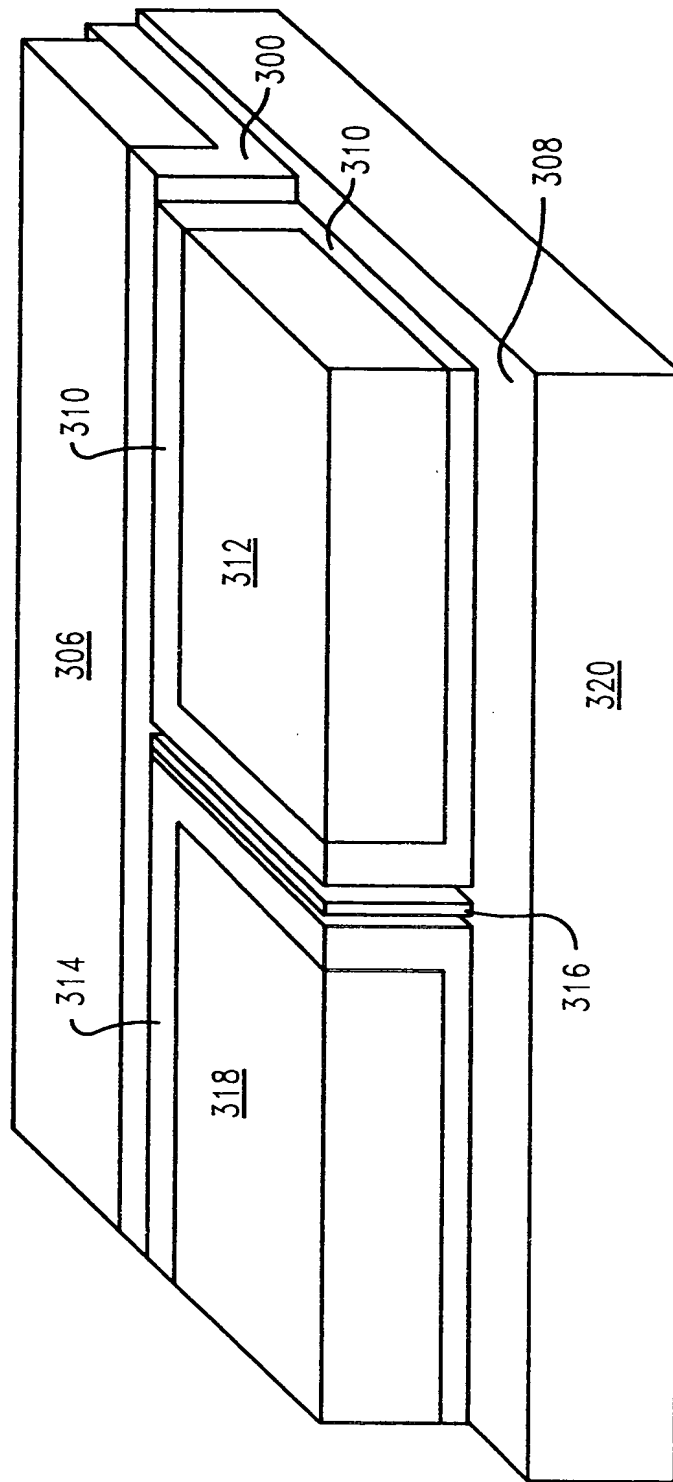


FIG. 10C

Replacement gate (dual metal)  
-> Poly- Si RIE back / CMP

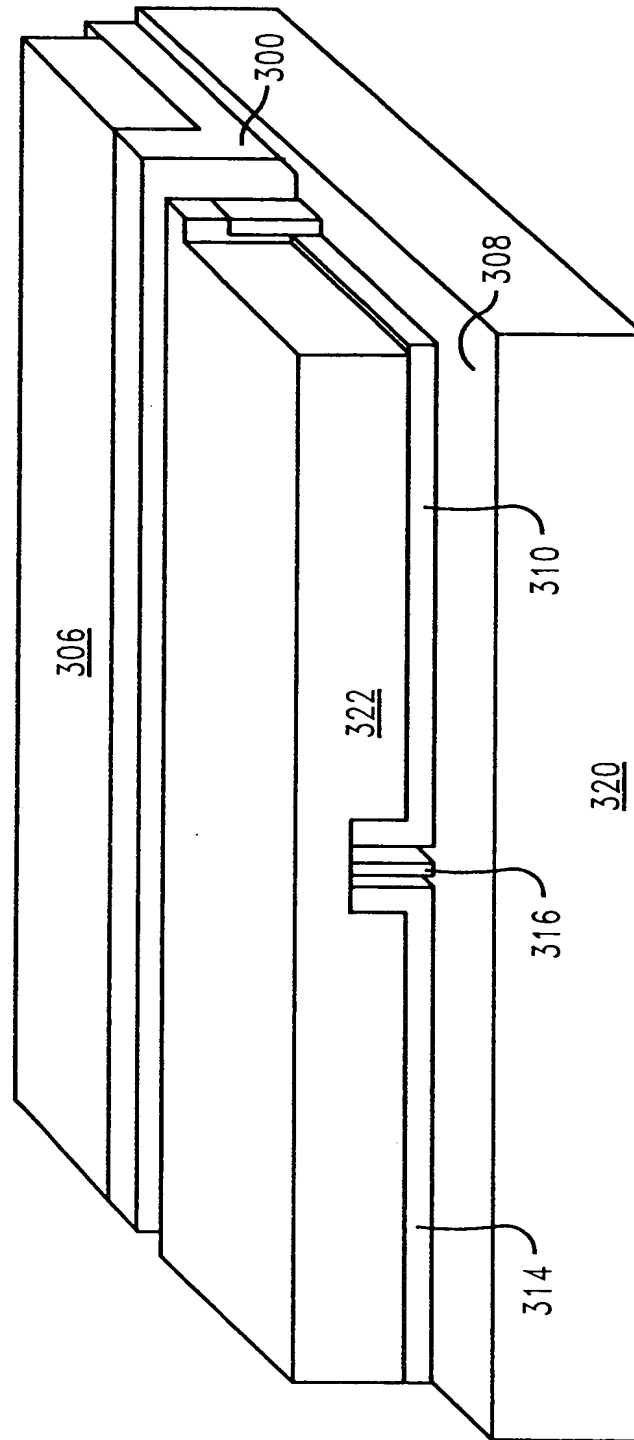


FIG. 10D

Replacement gate (dual metal)  
-> Co-silicidation

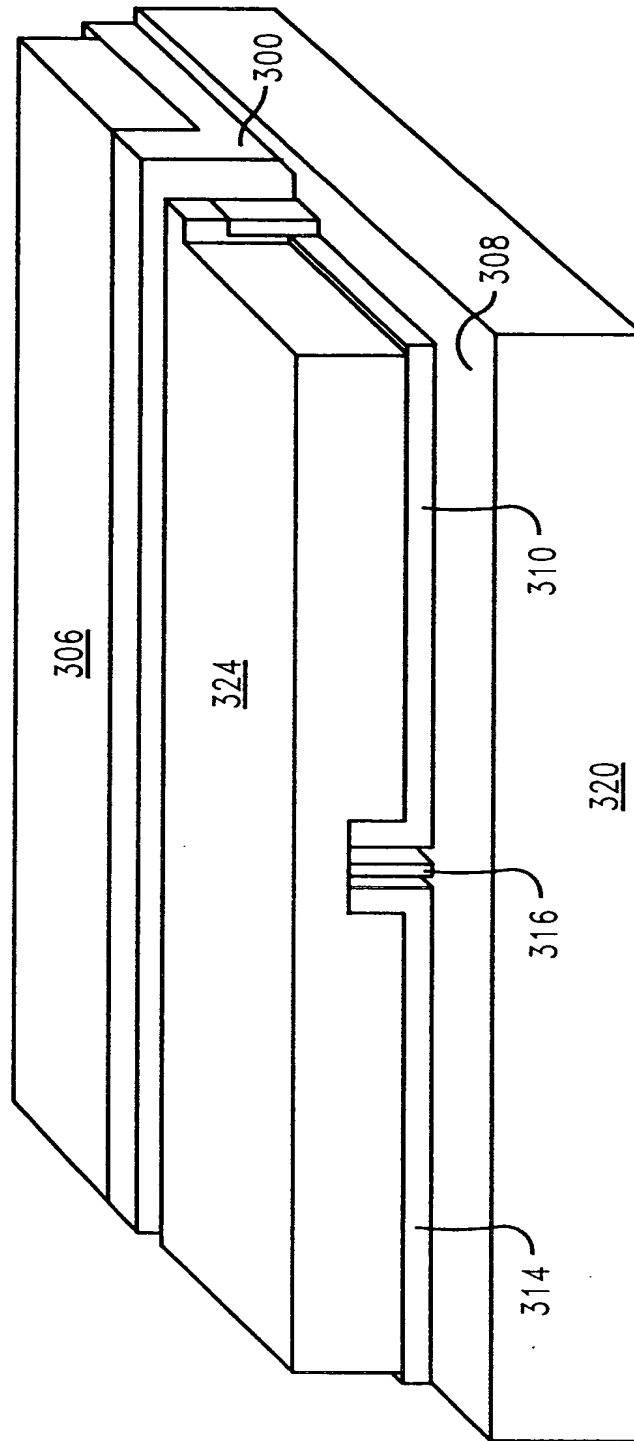


FIG. 10E